

(12) UK Patent Application (19) GB (11) 2 220 272 (13) A

(43) Date of A publication 04.01.1990

(21) Application No 8815417.4

(22) Date of filing 29.06.1988

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(51) INT CL'
G01R 31/28

(52) UK CL (Edition J)
G1U UC9C
H3T TBRB T2T3F T4D T4H2 T5E

(56) Documents cited
WO 84/03012 A1

(58) Field of search
UK CL (Edition J) G1U, G4A
INT CL' G01R, G06F, H03K

(54) Testing digital circuits

(57) To test a digital data storage circuit which includes two latch elements (5, 10) each formed by two complementary transistor inverter circuits S_1S_2 , S_3S_4 connected in a positive feedback arrangement and in which the output current capability of the second inverter circuit is restricted to enable the latch element to change state in response to input signals applied to it, a transistor (T_2) is blocked (6) and the first latch element (5) is connected in a two elements per bit shift register configuration with the second latch element (10) by series connected transistors (T_4 , T_5) controlled by antiphase square waves (T3T, H1T). During normal operation asynchronous SET and CLEAR signals are used to control three transistors (T_1 , T_2 , T_6) whereby to be able to apply (via T_3) one of two voltage levels to the first latch (5), one of the shift register transistors (T_4) being closed. Each latch (5, 10) may be as shown in Fig 2, the transistors being of differing size, as illustrated.

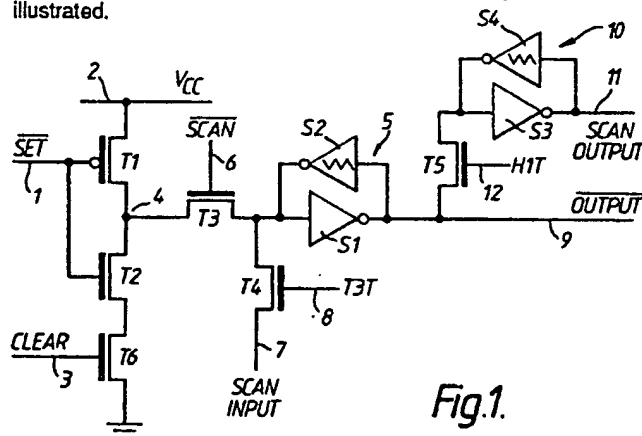


Fig.1.

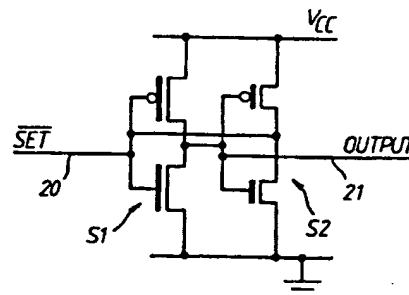


Fig.2.

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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IMPROVEMENTS IN OR RELATING TO INTEGRATED CIRCUITS

This invention relates to integrated circuits and in particular to a testable latch for latching asynchronous signals, the latch being suitable for use in an integrated circuit.

In the manufacture of microprocessors and other digital signal processors, it is essential to be able to test the functioning of the different parts of the circuit. The testing is typically achieved by providing in the processor an alternative set of interconnections between all the latches so that they are joined together to form a single shift register. In order to effect the testing a pattern of 1's and 0's is stepped in through the shift register connection to set the latches to known states. The microprocessor is then reconfigured to its normal functional connections and is caused to operate normally for at least one clock cycle. After that the data stored in the latches is stepped out along the shift register path and compared with the output expected. In this way failure of the microprocessor to perform the required logical operations can be detected and the likely cause of such failures pinpointed in the device. This test also enables the ability of the latches to store both the "1" state and the "0" state satisfactorily to be checked.

In order to implement this testing operation each latch in the microprocessor must be provided with selectable inputs, at least one for its normal operation and at least another for connecting the latches together in the shift register configuration.

Some latches in many microprocessors are intended to respond to asynchronous inputs, for example, inputs which arise from outside the device. An asynchronous input takes the form of a SET signal on one conductor defining the transition to the "1" state and a CLEAR signal on another conductor defining the transition to the "0" state.

Asynchronous signals are usually latched using a pair of cross-coupled NAND-gates to form a bistable element with separate SET and CLEAR inputs applied in inverted form to the two NAND-gates. Although it would be possible to connect such a latch into a shift register with other latches so that it could be tested in the manner described above, it would require a large amount of additional circuitry to provide the additional connections in the inputs to the latch required to produce the shift register configuration. Moreover, since the additional circuitry is required to produce the shift register configuration it cannot be tested independently of the latches.

It is an object of the present invention to provide a testable digital data storage circuit in which the above difficulties are substantially overcome.

According to a first aspect of the present invention there is provided a testable digital data storage circuit for use in an integrated circuit including first and second two-state latch elements each of which in use produces an output in the form of a selected one of two voltage levels depending only on whether an input signal applied to the particular element is above or below a threshold voltage, an input terminal for an input signal to the circuit, a first output terminal connected to the output of the first latch element, switch means responsive to asynchronous input signals to establish one of two voltage levels selectively, and first gating means connected to apply the voltage level established by the switch means to the input of the first latch element, wherein to enable the circuit to be tested second and third gating means are provided respectively connected from a test input terminal to the input of the first latch element and from the output of the first latch element to the input of the second latch element, the output of the second latch element being connected to a test output terminal, during normal operation the first gating means being maintained open to pass the voltage level to the first latch element and during testing the first gating means being closed and the second and third gating means being opened alternately.

According to a second aspect of the present invention there is provided a testable integrated circuit having a plurality of latch elements interconnected by logic circuits, at least one of the latch elements being adapted to receive asynchronous inputs, and in which for testing purposes the latch elements can be joined in a shift register configuration for entry and extraction of data bits, wherein the or each latch element which is adapted to receive asynchronous inputs in use produces an output in the form of one of two voltage levels depending only on whether a signal applied to an input terminal is above or below a threshold voltage and includes switch means responsive to the asynchronous inputs to apply a signal voltage above the threshold voltage or a signal voltage below the threshold voltage to the input terminal selectively.

The switch means may include a first transistor rendered conducting by a SET signal for conveying a first supply voltage to an output of the switch means and a second transistor rendered conducting by a CLEAR signal for conveying a second supply voltage different from the first supply voltage to the output of the switch means. The switch means may include a further transistor controlled by either the SET or CLEAR signal input connected in series with the second or first transistor so that the two supply voltages are not directly connected together if both the SET and CLEAR signals are present at the same time.

Each of the two-state latch elements may consist of a first complementary transistor inverter circuit connected to a second complementary transistor inverter circuit of restricted output current capability, the input of the latch element being connected to the input of the first inverter and the output of the latch element is connected to the output of the first inverter. The output of the second inverter serves to maintain the state, SET or RESET, into which the latch is switched by an input signal, and the restricted output current capability of the second inverter permits the state of the latch to be changed because it can be overridden by the current of an input signal applied to the input of the latch.

In the example to be described, the transistors are MOS transistors, but the circuit could be constructed using bipolar transistors or a mixture of bipolar and MOS transistors.

One example of a testable digital storage circuit will now be described with reference to the accompanying drawings, of which:-

FIGURE 1 is a circuit diagram of the example ; and

FIGURE 2 is the circuit diagram of one form of latch element which could be used in the example of Figure 1.

In Figure 1 a $\overline{\text{SET}}$ input on a conductor 1 is connected to the gates of a P-channel MOSFET T1 and an N-channel MOSFET T2. In accordance with convention a bar over the name of a signal, in this case SET, indicates that it is low when active. The channels of the transistors T1 and T2, which are their controlled current paths, are connected in series from a conductor 2, connected to a positive supply voltage VCC, to the channel of another N-channel MOSFET T6, the drain of which is connected to earth. The gate of the transistor T6 is connected to a conductor 3 to receive a CLEAR input signal. The signals $\overline{\text{SET}}$ and CLEAR come from an external source, for example, and consequently are asynchronous; that is to say, their timing is not necessarily related to that of the clock and other signals applied to the circuit. The junction 4 of the channels of the transistors T1 and T2 is connected through the channel of an N-channel MOSFET T3 to the input of a latch element 5. The gate of the transistor T3 is connected to a conductor 6 through which it receives a control signal $\overline{\text{SCAN}}$. The input of the latch element 5 is also connected through the channel of an N-channel MOSFET T4 to a conductor 7 from which it receives data from other latch elements when the latch elements are configured as a shift register. The gate of the transistor T4 is connected to a conductor 8 from which it receives a clock signal T3T.

The latch element 5 consists of an inverter S1 with a feedback inverter S2 connected from its output to its input. The inverter S2 has a restricted output current capability so as to permit the state of the latch element to be set by a

signal applied to its input. The output of the latch element is connected to a conductor 9 on which appears the output of the storage circuit in inverted form. The conductor 9 is connected to logic and/or other circuitry of a processor in which the storage circuit is built.

The conductor 9 is connected through the channel of an N-channel MOSFET T5 to the input of a second latch element 10, the output of which appears on a conductor 11 and is connected to the input of another storage circuit similar to that shown in Figure 1 to provide a connection between the storage circuits in the shift register configuration. The gate of the transistor 5 is connected to a conductor 1 on which appears a clock signal H1T. The latch element 10 consists of two inverters S3 and S4 connected in a similar way to the inverters S1 and S2 of the latch 5. The inverter S4 has a restricted output current capability.

In the normal operation of the circuit shown in Figure 1, the $\overline{\text{SCAN}}$ signal applied to the conductor 6 is high and the transistor T3 is conducting so that the input of the latch element 5 is connected to the junction 4 between the transistors T1 and T2. At this time the clock signal T3T is held low so that the transistor T4 is not conducting. Although the clock signal H1T is always present so that the output is transferred to the latch 10, this does not interfere with the normal operation of the circuit because the transistor T4 of the succeeding circuit is blocked. The signal $\overline{\text{SET}}$ from an external source, for example, when low will cause the transistor T1 to conduct and the transistor T2 to be non-conducting which would provide a high level at the junction 4 causing the output of the latch element 5 to go low. This output is conveyed by the conductor 9 to logic and/or other components not shown in Figure 1. The voltage at the junction 4 will be held low, that is to say, close to ground potential when the $\overline{\text{SET}}$ signal 1 is high and the CLEAR signal applied to the conductor 3 is also high, so that both transistors T2 and T6 are conducting. At this time the transistor T1 is not conducting. The provision of the transistor T2 in addition to the transistor T6 serves to

prevent an inadvertent short-circuiting of the supply conductor 2 to ground should the $\overline{\text{SET}}$ signal be low at the same time as the CLEAR signal is high. Instead of the transistor T2, a transistor rendered non-conducting by the CLEAR signal may be provided in series with the transistor T1.

When it is required to test the functioning of the processor of which the storage circuit shown in Figure 1 is a part, the latch elements 5 and 10 are connected in a shift register configuration with the latch elements of other storage circuits in the processor through the transistors T4 and T5. Because the clock signal H1T is always present the state of the latch element 10 always follows that of the latch element 5, which means that as soon as the clock T3T is started the latch element 5 receives the state of the preceding latch element 10 in the shift register. Since the timing of changes of state of the latch element 5 in response to the $\overline{\text{SET}}$ and CLEAR signals relative to the pulses of the clock signals H1T and T3T is not fixed it is possible that the latch element 5 will be changing state when the transistor T5 becomes conducting. The latch element 10, however, adopts either the "0" or the "1" state in response to the input it receives from the latch element 5, thereby avoiding the stepping of an indeterminate state along the shift register. When the latch elements are operated in a shift register configuration the $\overline{\text{SCAN}}$ input applied to the conductor 6 is low so that the normal input to the latch element 5 through the transistor T3 is disabled because the transistor T3 is held non-conducting. The clock signals T3T and H1T are square waves of opposite polarity so that when the transistor T4 is conducting the transistor T5 is non-conducting, and vice versa. A sequence of 1's and 0's is entered into the processor along the shift register formed by the latch elements such as 5 and 10 in each of the storage circuits of the processor. The shift register operates on a two elements per bit cycle. After the data bits are stored in the storage circuits as required, the operation of the shift register is stopped and the processor caused to operate

normally for at least one clock cycle by opening the transistors such as T3 again. When the operations required of the processor have been performed, the resulting data bits stored in the storage elements are then shifted out along the shift register path with the transistors such as T3 blocked. In this way the functioning of the logic and other circuits interconnecting the storage elements can be tested.

Figure 2 shows one example of the construction of a latch element using CMOS technology. In Figure 2, the input to the latch element is applied along conductor 20 and the output appears on a conductor 21. The element consists of two CMOS inverters, S1 and S2, corresponding to the components of the latch element 5 of Figure 1. As shown in Figure 2, the transistors of the inverter S2 are smaller than the transistors of the inverter S1, so that the output current capability of the inverter S2 is relatively restricted and can be overridden by the current of an input signal applied to the conductor 20. If the current were not so restricted, the inverter S2 would oppose any change to the voltage on the conductor 20 and it would not be possible to change the state of the latch element. On the other hand, the positive feedback provided by the inverter S2 serves to hold the latch element in the state to which it has been set.

The output current of the inverter S2 (and S4) may be restricted in other ways than using transistors that are smaller. For example, a resistor may be incorporated in the output connection of the inverter to restrict the current.

The latch elements may be of a different construction from that described provided that they can latch a state according to the level of a single input signal. It is not necessary for all of the latch elements to be of the same construction.

Although the digital data storage circuit has been described with reference to an example using MOS transistors, it could alternatively be constructed using bipolar transistors or a mixture of bipolar and MOS transistors.

The transistors T1, T2 and T6 may be replaced by other switch means responsive to the asynchronous SET and CLEAR signals, upright or inverted, and capable of applying the required logic signal levels to the latch element 5. Unless the signals SET and CLEAR are such that they cannot both be active at the same time, the switch means should be arranged so that the sources of the logic signal levels are not short-circuited when the signals SET and CLEAR are both active at the same time.

Each of the transistors T3, T4 and T5 may be replaced by another form of gate capable of transferring signal levels in the manner described above.

Different forms of switch means and gate may be used in different places in the circuit.

The digital data storage circuit described above has the advantage that it requires relatively few additional components to provide for the testing of the processor in which it is to be incorporated and that no combinatorial logic is included in the shift register.

WHAT WE CLAIM IS:

1. A testable digital data storage circuit for use in an integrated circuit including

first and second two-state latch elements each of which in use produces an output in the form of a selected one of two voltage levels depending only on whether an input signal applied to the particular element is above or below a threshold voltage,

an input terminal for an input signal to the circuit, a first output terminal connected to the output of the first latch element,

switch means responsive to asynchronous input signals to establish one of two voltage levels selectively, and

first gating means connected to apply the voltage level established by the switch means to the input of the first latch element,

wherein to enable the circuit to be tested second and third gating means are provided respectively connected from a test input terminal to the input of the first latch element and from the output of the first latch element to the input of the second latch element, the output of the second latch element being connected to a test output terminal, during normal operation the first gating means being maintained open to pass the voltage level to the first latch element and during testing the first gating means being closed and the second and third gating means being opened alternately.

2. A storage circuit according to claim 1 in which the switch means includes a first transistor rendered conducting by a SET signal and connected from a first supply conductor to the first gating means and a second transistor rendered conducting by a CLEAR signal and connected from a second supply conductor to the first gating means.

3. A storage circuit according to claim 2 in which the switch means includes a further transistor which is rendered non-conducting by either the SET signal or the CLEAR signal and which is connected in series with either the second transistor or the first transistor, so that the first and second supply conductors are not connected together when both the SET signal and the CLEAR are present at the same time.

4. A storage circuit according to any one of the preceding claims in which at least one of the gating means consists of a MOS transistor the controlled path of which is connected from the input to the output of the gating means.

5. A storage circuit according to any one of the preceding claims wherein each latch element includes first and second complementary transistor inverter circuits connected in a positive feedback loop, the second complementary transistor inverter circuit having a restricted output current capability.

6. A storage circuit according to any one of claims 2 to 5 wherein all the transistors are MOS transistors.

7. A storage circuit according to any one of claims 2 to 5 wherein all the transistors are bipolar transistors.

8. A storage circuit according to any one of claims 2 to 5 wherein at least one of the transistors is a MOS transistor and at least one other of the transistors is a bipolar transistor.

9. A digital data storage circuit substantially as described herein with reference to Figures 1 and 2.

10. A testable integrated circuit having a plurality of latch elements interconnected by logic circuits, at least one of the latch elements being adapted to receive asynchronous inputs, and in which for testing purposes the latch elements can be joined in a shift register configuration for entry and extraction of data bits, wherein the or each latch element which is adapted to receive asynchronous inputs in use produces an output in the form of one of two voltage levels depending only on whether a signal applied to an input terminal is above or below a threshold voltage and includes switch means responsive to the asynchronous inputs to apply a signal voltage above the threshold voltage or a signal voltage below the threshold voltage to the input terminal selectively.

11. A circuit according to claim 10 in which the switch means includes a first transistor rendered conducting by a SET signal and connected from a first supply conductor to the input terminal of the particular latch element and a second transistor rendered conducting by a CLEAR signal and connected from a second supply conductor to the input terminal of the particular latch element.

12. A circuit according to claim 11 in which the switch means includes a further transistor which is rendered non-conducting by either the SET signal or the CLEAR signal and which is connected in series with either the second transistor or the first transistor, so that the first and second supply conductors are not connected together when both the SET signal and the CLEAR are present at the same time.

13. A circuit according to any one of claims 10, 11 and 12 wherein each latch element has gating means arranged to block inputs to the particular latch element other than along the shift register during testing, and a plurality of further latch elements are provided respectively connected to receive the data from the first-mentioned latch elements, so that the shift register operates as a two elements per bit register.